



3 and 5 deg Camera electronics

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Introduction

Data Rates

Digitization time

Major steps

Outlook



Introduction

N channels 3 degree

- 1008 GAPDs
- 252 pixels

DRS sampling rate: f_s

- 1 GHz = 1 μ s
- 2 GHz = 500 ns
- 5 GHz = 200 ns

Event rate: f_{eve}

- 50 Hz ??

N channels 5 degree

- 2736 GAPDs
- 694 pixels

Time window for readout: t_r

- 10 ns?
- 100 ns?
- 500 ns?

Trigger efficiency t_{eff}

- 70 % ? 10 % ?

Occupancy

- (30 – 35) % ???

Number of samples: $N_s = f_s$ $\cdot t_r$

- 1 GHz * 10 ns = 10
- 2 GHz * 100 ns = 200
- Full DRS = 1024

Trigger rate: $f_t = f_{eve}/t_{eff}$

- 50 Hz / 10% = 500 Hz
- 50 Hz / 70% = 72 Hz



Event Size

Event size: bytes / sample * Nsamples * ftrigger * Nchannels

bytes / sample	Nsamples	ftrigger	Nchannels	event size	
2	10	72	694	1.0	MB
2	10	500	694	6.6	MB
2	100	72	694	9.5	MB
2	100	500	694	66.2	MB
2	1024	72	694	97.6	MB
2	1024	500	694	677.7	MB
2	10	72	2637	3.6	MB
2	10	500	2637	25.1	MB
2	100	72	2637	36.2	MB
2	100	500	2637	251.5	MB
2	1024	72	2637	370.8	MB
2	1024	500	2637	2575.2	MB

The most important parameter is the number of samples.

DRS4 region of interest ? Can different DRS4 chips be kept aligned in time?



Conversion Time (CT)

fADC ... sampling frequency of the ADC

NADC ... number of ADCs used

$CT = N_{\text{samples}} / f_{\text{ADC}} * N_{\text{channels}} / N_{\text{ADC}}$

Nsamples	fADC	NADC	Nchannels	DT in ms
10	40	1	694	0.1735
10	200	1	694	0.0347
100	40	1	694	1.735
100	200	1	694	0.347
1024	40	1	694	17.7664
1024	200	1	694	3.55328
10	40	19	694	0.009131579
10	200	19	694	0.001826316
100	40	19	694	0.091315789
100	200	19	694	0.018263158
1024	40	19	694	0.935073684
1024	200	19	694	0.187014737

This does not take into account other delays: DRS start-stop, multiplexing, ...



Major steps

Analog signal processing

- Pre-amplifier
- Shaper (if needed), Clipping (if wanted)
- Signal extraction for trigger primitives (analog)

Data sampling and buffering

- Analog pipeline (DRS 4, others?) or Digital pipeline
- Delay line

Digitization

- ADC (multiplexed)
- FADC?

Digital Signal handling

- FPGA?

Data transmission camera – counting hut

- Analog or digital data
- Optical or electrical signals

Signal processing and storage

- Some standard:
 - VME? CAMAC? PC?



What has to be done?

In addition a trigger must be generated

Where are the
necessary processing
steps happening

- Camera module or Counting hut?
- Signal delay over 25m ~ 125 ns \rightarrow trigger in the counting hut and pipeline in the camera: 250 ns
- Analog signal processing must happen in the camera

Presently

- Pipeline, digitization and trigger generation in the counting hut

Simple approach

- Digitization and Pipeline in the camera
- Trigger generation in the camera
- Digital data transmission

Options?

- Analog pipeline in the camera + analog optical links?
- TPG in the camera + Trigger in the counting hut?

Should the system be able to handle multiple events? Requires intermediate buffers



Outlook

Analog electronics

- Depends on the geometry, a new geometry will very likely cause a re-desine
- trigger primitives generation if foreseen in the camera

Digital electronics 3 deg camera

- Can be copied from M0 (time vs. cost)

Digital electronics 5 deg camera

- Requires higher level of integration into the camera
- Based on DRS4 ?

Trigger

- To be integrated into the camera ? → to be designed
- In the counting hut? → timeing, number of channels and data transmission...

This effort must be shared within the collaboration